

### REMARKS

The applicant thanks the examiner for his review of the claims and prior art, and requests reconsideration of the pending claims in view of the below comments.

The office action rejected claims 2, 10, and 18 as being indefinite for failing to particularly point out and distinctly claim the subject matter the applicant regards as the invention. In response, the applicant amended those claims to show more clearly that they are controlled to operate with the same phase and duty cycles.

Claims 1-3 and 6-20 were rejected as being anticipated by U.S. patent number 4,170,740 (Pernyeszi).

In summary, claim 1 defines a multi-stage circuit having a first stage with an output switch, and a second stage with an input switch. The circuit also has a bootstrap module in communication with both switches. As discussed below, Pernyeszi does not disclose such first and second stages. Instead, figure 1 generally shows output terminals 52 and 54 with no connections.

More specifically, figure 1 of Pernyeszi shows a circuit 10 for delivering high voltage signals to an output having ports 52 and 54. The circuit 10 can be used in a system shown in figure 2, in which the circuit 10 can be substituted for switches S1-S6 (see column 4, line 67 to column 5, line 5). Clearly, two stages are not shown or suggested as being coupled with the output terminal 52 or 54, respectively. In fact, the office action could show no such stages. Accordingly, for this reason alone, all of the claims are allowable.

To expedite prosecution, however, the applicant has amended claims 1 and 8 to also require that the first stage have an amplifier with an amplifier output. This amplifier output is coupled with and drives a common node of the switches. As an example of this architecture, see figure 2, which shows the (-) output of the amplifier in the SHA stage driving and coupling with the common node between switches S3A and S3B.

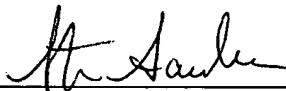
Pernyeszi clearly does not teach such an arrangement. Instead, the common node between the switches 48 and 50 are coupled with a floating voltage that is not

from an amplifier. Accordingly, for this additional reason, claims 1 and 8 are patentable over the cited art. In a similar manner, dependent claims 2-7, 9-14, and new dependent claim 29 also are allowable for the same reasons.

Claim 15 also is allowable for additional reasons other than those noted above. Specifically, in a manner similar to claim 1, claim 15 defines a multi-stage circuit. However, the defined circuit is a switched capacitor circuit. Pernyeszi does not teach or suggest such a circuit. In addition, claim 15 also defines a first stage having an output feedback loop. Again, Pernyeszi does not teach or suggest feedback from the output of any stage. Accordingly, for these and other reasons, claim 15 is allowable over the cited art. Claims 16-20 also are allowable for the same reasons.

This patent application therefore is in condition for allowance, and such action is respectfully solicited. The applicant's attorney, Steven Saunders, would welcome a telephone call from the examiner for any reason related to prosecution of this patent application.

Respectfully submitted,

By   
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